Contents

Fixed Virtual Platform

To develop ahead of hardware availability and to explore the design from a software perspective, the Fixed Virtual Platform (FVP) models many of the Arm IP in the Corstone SSE-310 design.

1.1 About the FVP

The Corstone SSE-310 FVP models a r0p0 version of Corstone SSE-310 Subsystem.

The FVP models the following IP components:

- Single Arm Cortex-M Olympus processor with MVE extension
- Single Arm Ethos-U55 processor
- Memory Protection Controller (MPC)
- Peripheral Protection Controller (PPC)
- Implementation Defined Attribution Unit (IDAU)

The FVP does not model every component that Corstone SSE-310 describes. For example, it does not model the CoreSight technology components.

The full description of components that are internal to the SSE-310 Subsystem can be found in the SSE-310 Example Subsystem TRM. The Corstone SSE-310 FVP drives system architecture and software standardization. The model provides software and binaries of proprietary firmware that reduce the amount of work that is required for SoC development.

1.2 Memory Map Overview

This memory map includes information regarding IDAU security information for memory regions. This table outlines the main FVP memories and their positions within the memory map.

Table 1-1 Memory Map overview

ROW ID	Address		Size	Description	Alias with Row ID	IDAU Region Values		
	From	To				Security	IDAUID	NSC
1	0x0000_0000	0x0000_7FFF	32KB	ITCM[3]	5	NS	0	0
2	0x0000_8000	0x00FF_FFFF	15.9MB	Reserved				
3	0x0100_0000	0x011F_FFFF	2MB	SRAM (2MB)[1]	7			
4	0x0120_0000	0x0FFF_FFFF	238MB	Reserved				
5	0x1000_0000	0x1000_7FFF	32KB	ITCM[3]	1	S	1	CODE NSC
6	0x1000_8000	0x10FF_FFFF	15.9MB	Reserved				

7	0x1100_0000	0x111F_FFFF	2MB	SRAM (2MB) [1]	3			
8	0x1120_0000	0x1FFF_FFFF	238MB	Reserved				
9	0x2000_0000	0x2000_7FFF	32KB	DTCM (4 x banks of 8KB)[3]	15	NS	2	0
10	0x2000_8000	0x20FF_FFFF	15.9MB	Reserved				
11	0x2100_0000	0x213F_FFFF	4MB	Internal SRAM Area (SSE-310 implements 2x2MB)[3]	17			
12	0x2140_0000	0x27FF_FFFF	108MB	Reserved				
13	0x2800_0000	0x287F_FFFF	8MB	QSPI (only 8MB) [1]	19			
14	0x2880_0000	0x2FFF_FFFF	120MB	Reserved				
15	0x3000_0000	0x3000_7FFF	32KB	DTCM (4 x banks of 8KB)[3]	9	S	3	RAM NSC
16	0x3000_8000	0x30FF_FFFF	15.9MB	Reserved				
17	0x3100_0000	0x313F_FFFF	4MB	Internal SRAM Area (SSE-310 implements 2x2MB)[3]	11			
18	0x3140_0000	0x37FF_FFFF	108MB	Reserved				
19	0x3800_0000	0x387F_FFFF	8MB	QSPI (only 8MB) [1]	13			
20	0x3880_0000	0x3FFF_FFFF	120MB	Reserved				
21	0x4000_0000	0x47FF_FFFF	128MB	Non-Secure Low Latency Peripheral Region.	23	NS	4	0
22	0x4800_0000	0x4FFF_FFFF	128MB	Non-Secure High Latency Peripheral Region.	24	NS	4	0
23	0x5000_0000	0x57FF_FFFF	128MB	Secure Low Latency Peripheral Region.	21	S	5	0
24	0x5800_0000	0x5FFF_FFFF	128MB	Secure High Latency Peripheral Region.	22	S	5	0
25	0x6000_0000	0x6FFF_FFFF	256MB	DDR4[1]		NS	6	0
26	0x7000_0000	0x7FFF_FFFF	256MB	DDR4[1]		S	7	0
27	0x8000_0000	0x8FFF_FFFF	256MB	DDR4[1]		NS	8	0
28	0x9000_0000	0x9FFF_FFFF	256MB	DDR4[1]		S	9	0
29	0xA000_0000	0xAFFF_FFFF	256MB	DDR4[1]		NS	A	0
30	0xB000_0000	0xBFFF_FFFF	256MB	DDR4[1]		S	B	0
31	0xC000_0000	0xCFFF_FFFF	256MB	DDR4[1]		NS	C	0
32	0xD000_0000	0xDFFF_FFFF	256MB	DDR4[1]		S	D	0
33	0xE000_0000	0xE00F_FFFF	1MB	External Private Peripheral Bus			Exempt	
34	0xE010_0000	0xE01F_FFFF	1MB	Reserved		NS	E	0
35	0xE020_0000	0xEFFF_FFFF	254MB	Maps to HMSTEXPPILL Expansion Interface[2]		NS	E	0
36	0xF000_0000	0xF00F_FFFF	1MB	Reserved			Exempt	
37	0xF010_0000	0xF01F_FFFF	1MB	Reserved		S	F	0
38	0xF020_0000	0xFFFF_FFFF	254MB	Maps to HMSTEXPPILL Expansion Interface[2]		S	F	0

Note[1] : Security Access is controlled by MPC.
Note[2] : Accesses to these addresses results in an AHB5 error response.
Note[3] : For security settings, control and features please refer to the Arm® Corstone™ SSE-310 Documentation.

1.3 FVP Peripherals

The Corstone SSE-310 includes peripherals that the software payload requires to run.

These peripherals are organized in following layer:

- Subsystem – The subsystem peripherals represent peripherals that are present on the SoC.
- Board - The board peripherals represent peripherals that may be present on the board onto which the SoC is mounted. The Corstone SSE-310 board model is based on the ARM MPS3 Board.

All peripherals that are extensions to the Corstone SSE-310 Subsystem are mapped into two key areas of the memory map:

- 0x4000_0000 to 0x47FF_FFFF and 0x4800_0000 to 0x4FFF_FFFF Non-Secure region which maps to AHB Master Expansion 1 interface.
- 0x5000_0000 to 0x57FF_FFFF and 0x5800_0000 to 0x5FFF_FFFF Secure region which maps to AHB Master Expansion 1 interface.

1.3.1 Subsystem Peripheral Memory Map

Table 1-2 Subsystem peripherals – Nonsecure

ROW ID	Address		Size	Description	Modelled in FVP
	From	To			
Non-Secure Region					
1	0x4000_0000	0x4000_0FFF	4KB	MHU 0	Not Modelled
2	0x4000_1000	0x4000_1FFF	4KB	MHU 1	Not Modelled
3	0x4000_2000	0x4000_3FFF	8KB	DMA	DMA-350
4	0x4000_4000	0x4000_4FFF	4KB	NPU APB	Modelled
	0x4000_5000	0x4001_EFFF		Reserved	
5	0x4001_F000	0x4001_FFFF	4KB	CPUID	Modelled
	0x4002_0000	0x4007_0000		Reserved	
6	0x4008_0000	0x4008_0FFF	4KB	Non-secure Access Configuration Registers	Modelled
	0x4008_1000	0x4008_FFFF		Reserved	
7	0x4009_0000	0x4009_3FFF	16KB	CryptoCell312	Not Modelled
	0x4009_4000	0x400F_FFFF		Reserved	
	0x4010_0000	0x47FF_FFFF		Board peripherals	
8	0x4800_0000	0x4800_0FFF	4KB	Timer 0	Modelled
9	0x4800_1000	0x4800_1FFF	4KB	Timer 1	Modelled
10	0x4800_2000	0x4800_2FFF	4KB	Timer 2	Modelled

11	0x4800_3000	0x4800_3FFF	4KB	Timer 3	Modelled
	0x4800_4000	0x4801_FFFF		Reserved	
12	0x4802_0000	0x4802_0FFF	4KB	SYSINFO	Modelled
	0x4802_1FFF	0x4802_EFFF		Reserved	
13	0x4802_F000	0x4802_FFFF	4KB	SLOWCLK Timer	Modelled
	0x4803_0000	0x4803_FFFF		Reserved	
14	0x4804_0000	0x4804_0FFF	4KB	Non-Secure Watchdog Control Frame	Modelled
15	0x4804_1000	0x4804_1FFF	4KB	Non-Secure Watchdog Refresh Frame	Modelled
	0x4804_2000	0x480F_FFFF		Reserved	

Table 1-3 Subsystem peripherals – Secure

ROW ID	Address		Size	Description	Modelled in FVP
	From	To			
Secure Region					
1	0x5000_0000	0x5000_0FFF	4KB	MHU 0	Not Modelled
2	0x5000_1000	0x5000_1FFF	4KB	MHU 1	Not Modelled
3	0x5000_2000	0x5000_3FFF	8KB	DMA	DMA-350
4	0x5000_4000	0x5000_4FFF	4KB	NPU APB	Modelled
	0x5000_5000	0x5001_EFFF		Reserved	
5	0x5001_F000	0x5001_FFFF	4KB	CPUID	Modelled
	0x5002_0000	0x5007_0000		Reserved	
6	0x5008_0000	0x5008_0FFF	4KB	Secure Access Configuration Registers	Modelled
	0x5008_1000	0x5008_2FFF		Reserved	
7	0x5008_3000	0x5008_3FFF	4KB	Internal SRAM MPC 0	Modelled
8	0x5008_4000	0x5008_4FFF	4KB	Internal SRAM MPC 1	Modelled
	0x5008_5000	0x5008_FFFF		Reserved	
9	0x5009_0000	0x5009_3FFF	16KB	CryptoCell312	Not Modelled
	0x5009_4000	0x500F_FFFF		Reserved	
	0x5010_0000	0x57FF_FFFF		Board peripherals	
10	0x5800_0000	0x5800_0FFF	4KB	Timer 0	Modelled
11	0x5800_1000	0x5800_1FFF	4KB	Timer 1	Modelled
12	0x5800_2000	0x5800_2FFF	4KB	Timer 2	Modelled
13	0x5800_3000	0x5800_3FFF	4KB	Timer 3	Modelled
	0x5800_4000	0x5801_FFFF		Reserved	

14	0x5802_0000	0x5802_0FFF	4KB	SYSINFO	Modelled
15	0x5802_1000	0x5802_1FFF	4KB	SYSCONTROL	Modelled
16	0x5802_2000	0x5802_2FFF	4KB	SYS_PPU	Modelled
17	0x5802_3000	0x5802_3FFF	4KB	CPU0_PPU	Modelled
	0x5802_4000	0x5802_6FFF		Reserved	
18	0x5802_7000	0x5802_7FFF	4KB	CRYPTO_PPU	Not Modelled
19	0x5802_8000	0x5802_8FFF	4KB	MGMT_PPU	Modelled
20	0x5802_9000	0x5802_9FFF	4KB	DBG_PPU	Modelled
21	0x5802_A000	0x5802_AFFF	4KB	NPU_PPU	Modelled
	0x5802_B000	0x5802_DFFF		Reserved	
22	0x5802_E000	0x5802_EFFF	4KB	SLOWCLK Watchdog	Modelled
23	0x5802_F000	0x5802_FFFF	4KB	SLOWCLK Timer	Modelled
	0x5803_0000	0x5803_FFFF		Reserved	
24	0x5804_0000	0x4804_0FFF	4KB	Secure Watchdog Control Frame	Modelled
25	0x5804_1000	0x4804_1FFF	4KB	Secure Watchdog Refresh Frame	Modelled
	0x5804_2000	0x580F_FFFF		Reserved	

1.3.2 Expansion Peripheral Memory Map

Table 1-4 Board peripherals – Nonsecure

ROW ID	Address		Size	Description	Modelled in FVP
	From	To			
Non-Secure Region					
1	0x4110_0000	0x4110_0FFF	4KB	GPIO 0	CMSDK GPIO
2	0x4110_1000	0x4110_1FFF	4KB	GPIO 1	CMSDK GPIO
3	0x4110_2000	0x4110_2FFF	4KB	GPIO 2	CMSDK GPIO
4	0x4110_3000	0x4110_3FFF	4KB	GPIO 3	CMSDK GPIO
5	0x4110_4000	0x4110_4FFF	4KB	USER AHB 0	Not Modelled
6	0x4110_5000	0x4110_5FFF	4KB	USER AHB 1	Not Modelled
7	0x4110_6000	0x4110_6FFF	4KB	USER AHB 2	Not Modelled
8	0x4110_7000	0x4110_7FFF	4KB	USER AHB 3	Not Modelled
	0x4110_8000	0x413F_FFFF		Reserved	
9	0x4140_0000	0x414F_FFFF	1MB	Ethernet	SMSC91C111 Ethernet controller
10	0x4150_0000	0x415F_FFFF	1MB	USB	Dummy Stub
	0x4160_0000	0x416F_FFFF		Reserved	
11	0x4170_0000	0x4170_0FFF	4KB	User APB0	Not Modelled
12	0x4170_1000	0x4170_1FFF	4KB	User APB1	Not Modelled
13	0x4170_2000	0x4170_2FFF	4KB	User APB2	Not Modelled
14	0x4170_3000	0x4170_3FFF	4KB	User APB3	Not Modelled

	0x4170_4000	0x417F_FFFF		Reserved	
15	0x4180_0000	0x4180_0FFF	4KB	QSPI Config	Not Modelled
16	0x4180_1000	0x4180_1FFF	4KB	QSPI Write	Not Modelled
	0x4180_2000	0x47FF_FFFF		Reserved	
	0x4800_0000	0x480F_FFFF		Subsystem peripherals	
17	0x4810_3000	0x4810_31FF	0.5KB	U55 timing adapter 0 APB	Modelled
18	0x4810_3200	0x4810_33FF	0.5KB	U55 timing adapter 1 APB	Modelled
	0x4810_3400	0x491F_FFFF		Reserved	
19	0x4920_0000	0x4920_0FFF	4KB	FPGA - SBCon I2C (Touch)	Partial modelled
20	0x4920_1000	0x4920_1FFF	4KB	FPGA - SBCon I2C (Audio Conf)	Dummy Stub
21	0x4920_2000	0x4920_2FFF	4KB	FPGA - PL022 (SPI ADC)	Dummy Stub
22	0x4920_3000	0x4920_3FFF	4KB	FPGA - PL022 (SPI Shield0)	Dummy Stub
23	0x4920_4000	0x4920_4FFF	4KB	FPGA - PL022 (SPI Shield1)	Dummy Stub
24	0x4920_5000	0x4920_5FFF	4KB	SBCon (I2C - Shield0)	Dummy Stub
25	0x4920_6000	0x4920_6FFF	4KB	SBCon (I2C – Shield1)	Dummy Stub
26	0x4920_7000	0x4920_7FFF	4KB	USER APB	Dummy Stub
27	0x4920_8000	0x4920_8FFF	4KB	FPGA - SBCon I2C (DDR4 EEPROM)	Dummy Stub
	0x4920_9000	0x492F_FFFF		Reserved	
28	0x4930_0000	0x4930_0FFF	4KB	FPGA - SCC registers	Modelled
29	0x4930_1000	0x4930_1FFF	4KB	FPGA - I2S (Audio)	Partial modelled
30	0x4930_2000	0x4930_2FFF	4KB	FPGA - IO (System Ctrl + I/O)	Modelled
31	0x4930_3000	0x4930_3FFF	4KB	UART0 - UART_F [0]	CMSDK UART
32	0x4930_4000	0x4930_4FFF	4KB	UART1 - UART_F [1]	CMSDK UART
33	0x4930_5000	0x4930_5FFF	4KB	UART2 - UART_F [2]	CMSDK UART
34	0x4930_6000	0x4930_6FFF	4KB	UART3 - UART Shield 0	Dummy Stub
35	0x4930_7000	0x4930_7FFF	4KB	UART4 - UART Shield 1	Dummy Stub
36	0x4930_8000	0x4930_8FFF	4KB	UART5 - UART_F [3]	CMSDK UART
	0x4930_9000	0x4930_9FFF	4KB	Reserved	
37	0x4930_A000	0x4930_AFFF	4KB	CLCD Config Reg	Partial modelled
37	0x4930_B000	0x4930_BFFF	4KB	RTC	PL031_RTC

Table 1-5- Board peripherals – Secure

ROW ID	Address		Size	Description	Modelled in FVP
	From	To			
Secure Region					
1	0x5110_0000	0x5110_0FFF	4KB	GPIO 0	CMSDK GPIO
2	0x5110_1000	0x5110_1FFF	4KB	GPIO 1	CMSDK GPIO
3	0x5110_2000	0x5110_2FFF	4KB	GPIO 2	CMSDK GPIO
4	0x5110_3000	0x5110_3FFF	4KB	GPIO 3	CMSDK GPIO
5	0x5110_4000	0x5110_4FFF	4KB	USER AHB 0	Not Modelled
6	0x5110_5000	0x5110_5FFF	4KB	USER AHB 1	Not Modelled
7	0x5110_6000	0x5110_6FFF	4KB	USER AHB 2	Not Modelled
8	0x5110_7000	0x5110_7FFF	4KB	USER AHB 3	Not Modelled
	0x5110_8000	0x513F_FFFF		Reserved	
9	0x5140_0000	0x514F_FFFF	1M	Ethernet	SMSC91C111 Ethernet controller
10	0x5150_0000	0x515F_FFFF	1M	USB	Dummy Stub
	0x5160_0000	0x516F_FFFF		Reserved	
11	0x5170_0000	0x5170_0FFF	4KB	User APB0	Not Modelled
12	0x5170_1000	0x5170_1FFF	4KB	User APB1	Not Modelled
13	0x5170_2000	0x5170_2FFF	4KB	User APB2	Not Modelled
14	0x5170_3000	0x5170_3FFF	4KB	User APB3	Not Modelled
	0x5170_4000	0x517F_FFFF		Reserved	
15	0x5180_0000	0x5180_0FFF	4KB	QSPI Config	Not Modelled
16	0x5180_1000	0x5180_1FFF	4KB	QSPI Write	Not Modelled
	0x5180_2000	0x56FF_FFFF		Reserved	
17	0x5700_000	0x5700_0FFF	4KB	SRAM Memory Protection Controller (MPC)	Modelled
18	0x5700_1000	0x5700_1FFF	4KB	QSPI Memory Protection Controller (MPC)	Modelled
19	0x5700_2000	0x5700_2FFF	4KB	DDR4 Memory Protection Controller (MPC)	Modelled
	0x5700_3000	0x57FF_FFFF		Reserved	
	0x5800_0000	0x580F_FFFF		Subsystem peripherals	
20	0x5810_3000	0x5810_31FF	0.5KB	U55 timing adapter 0 APB	Modelled
21	0x5810_3200	0x5810_33FF	0.5KB	U55 timing adapter 1 APB	Modelled
	0x5810_3400	0x591F_FFFF		Reserved	
22	0x5920_4000	0x5920_4FFF	4KB	FPGA - PL022 (SPI Shield1)	Dummy Stub
23	0x5920_5000	0x5920_5FFF	4KB	SBCon (I2C - Shield0)	Dummy Stub
24	0x5920_6000	0x5920_6FFF	4KB	SBCon (I2C - Shield1)	Dummy Stub
25	0x5920_7000	0x5920_7FFF	4KB	USER APB	Dummy Stub
26	0x5920_8000	0x5920_8FFF	4KB	DDR4 EEPROM	Dummy Stub
	0x5920_9000	0x592F_FFFF		Reserved	
27	0x5930_0000	0x5930_0FFF	4KB	FPGA - SCC registers	Modelled

28	0x5930_1000	0x5930_1FFF	4KB	FPGA - I2S (Audio)	Partial modelled
29	0x5930_2000	0x5930_2FFF	4KB	FPGA - IO (System Ctrl + I/O)	Modelled
30	0x5930_3000	0x5930_3FFF	4KB	UART0 - UART_F [0]	CMSDK UART
31	0x5930_4000	0x5930_4FFF	4KB	UART1 - UART_F [1]	CMSDK UART
32	0x5930_5000	0x5930_5FFF	4KB	UART2 - UART_F [2]	CMSDK UART
33	0x5930_6000	0x5930_6FFF	4KB	UART3 - UART Shield 0	Dummy Stub
34	0x5930_7000	0x5930_7FFF	4KB	UART4 - UART Shield 1	Dummy Stub
35	0x5930_8000	0x5930_8FFF	4KB	UART5 - UART_F [3]	CMSDK UART
	0x5930_9000	0x5930_9FFF	4KB	Reserved	
36	0x5930_A000	0x5930_AFFF	4KB	CLCD Config Reg	Partial modelled
37	0x5930_B000	0x5930_BFFF	4KB	RTC	PL031_RTC

1.3.3 Expansion Peripheral Interrupt Map

Table 1-6- Interrupt map at the board layer

Interrupt Input	Interrupt Source	Description
IRQ [32]	System timestamp counter interrupt	Not implemented
IRQ [33]	UART 0 Receive Interrupt	
IRQ [34]	UART 0 Transmit Interrupt	
IRQ [35]	UART 1 Receive Interrupt	
IRQ [36]	UART 1 Transmit Interrupt	
IRQ [37]	UART 2 Receive Interrupt	
IRQ [38]	UART 2 Transmit Interrupt	
IRQ [39]	UART 3 Receive Interrupt	
IRQ [40]	UART 3 Transmit Interrupt	
IRQ [41]	UART 4 Receive Interrupt	
IRQ [42]	UART 4 Transmit Interrupt	
IRQ [43]	UART 0 Combined Interrupt	
IRQ [44]	UART 1 Combined Interrupt	
IRQ [45]	UART 2 Combined Interrupt	
IRQ [46]	UART 3 Combined Interrupt	
IRQ [47]	UART 4 Combined Interrupt	
IRQ [48]	UART Overflow (0, 1, 2, 3, 4 & 5)	
IRQ [49]	Ethernet	
IRQ [50]	Audio I2S	
IRQ [51]	Touch Screen	
IRQ [52]	USB	
IRQ [53]	SPI ADC	
IRQ [54]	SPI (Shield 0)	
IRQ [55]	SPI (Shield 1)	
IRQ [56]	Reserved	
IRQ [57]	DMA Channel 0 Interrupt	
IRQ [58]	DMA Channel 1 Interrupt	
IRQ [68:59]	Reserved	
IRQ [69]	GPIO 0 Combined Interrupt	
IRQ [70]	GPIO 1 Combined Interrupt	
IRQ [71]	GPIO 2 Combined Interrupt	
IRQ [72]	GPIO 3 Combined Interrupt	
IRQ [88:73]	GPIO 0 individual interrupts	
IRQ [104:89]	GPIO 1 individual interrupts	
IRQ [120:105]	GPIO 2 individual interrupts	
IRQ [124:121]	GPIO 3 individual interrupts	
IRQ [125]	UART 5 Receive Interrupt	

IRQ [126]	UART 5 Transmit Interrupt	
IRQ [127]	UART 5 Combined Interrupt	
IRQ [130:128]	Reserved	

1.4 Peripheral Protection Controller Expansion Map

The Corstone SSE-310 FVP implements Secure Access configuration registers which controls security and privileged accesses to peripherals connected to PPC.

Table 1-7- Secure Access configuration registers- PPC bits

Bit	MAIN_PPCEXP0 (AHB0)	MAIN_PPCEXP1 (AHB1)	PERIPH_PPCEXP0 (APB0)	PERIPH_PPCEXP1 (APB1)	PERIPH_PPCEXP2 (APB2)
0	GPIO-0			SBCon I2C (Touch Screen)	FPGA - SCC registers
1	GPIO-1			SBCon I2C (Audio Conf)	FPGA - I2S (Audio)
2	GPIO-2			FPGA PL022 (SPI2 for ADC)	FPGA – GPIO (System Ctrl + I/O)
3	GPIO-3			FPGA PL022 (SPI Shield0)	UART0
4	User AHB 0			FPGA PL022 (SPI Shield1)	UART1
5	User AHB 1		U55 APB (Timing Adapters)	FPGA SBCon (I2C - Shield0)	UART2
6	User AHB 2			FPGA SBCon (I2C – Shield1)	UART3 STUB
7	User AHB 3			Reserved	UART4 STUB
8	USB and Ethernet			FPGA – SBCon I2C (DDR4 EPROM)	UART5
9					Reserved
10					CLCD Config Reg
11					RTC
12					
13			SRAM MPC		
14			QSPI MPC		
15			DDR MPC		
PPC IRQ No.	5	6	2	3	4

1.5 Memory Components

The Corstone SSE-310 FVP also includes following memory components and their Security Access is controlled by MPC.

Table 1-8- Memory Components

Name	Non-secure	Secure alias	Size
SRAM	0x0100_0000 - 0x011F_FFFF	0x1100_0000 - 0x111F_FFFF	2MB
QSPI SRAM	0x2800_0000 - 0x287F_FFFF	0x3800_0000 - 0x387F_FFFF	8MB
DDR0	0x6000_0000 - 0x6FFF_FFFF	0x7000_0000 - 0x7FFF_FFFF	256MB
DDR1	0x8000_0000 - 0x8FFF_FFFF	0x9000_0000 - 0x9FFF_FFFF	256MB
DDR2	0xA000_0000 - 0xAFFF_FFFF	0xB000_0000 - 0xBFFF_FFFF	256MB
DDR3	0xC000_0000 - 0xCFFF_FFFF	0xD000_0000 - 0xDFFF_FFFF	256MB

Note

Some of the MPS3 Fast Models have minimal implementations, for more information refer documents in FVP package.

Note

The FVP is used with the Corstone SEE-310 software package. See the Corstone SSE-310 Software Bundle Readme *for instructions on how to set up and run the FVP.*

1.6 Limitations

1. QSPI is not modelled, we have QSPI SRAM instead.
2. Dummy Stub – These stubs have minimal implementation. Models with dummy APB will have memory access.
3. Partial Modelled – Certain features are implemented. Refer documents mentioned in section 1.7 for further information.

1.7 Other documents

See the following documents for other relevant information:

- Arm® Corstone™ SSE-300 Example Subsystem Technical Reference Manual
- Arm® MPS3 FPGA Prototyping Board Technical Reference Manual
- Corstone-300 – Arm Developer